L27: Entry 8 of 25 File: USPT May 15, 2001

DOCUMENT-IDENTIFIER: US 6233717 B1
TITLE: Multi-bit memory device having error check and correction circuit and method for checking and correcting data errors therein

Brief Summary Text (25):
These and other objects, advantages and features of the present invention are provided by storing normal data information into a plurality of first memory cells (i.e., multibit memory cells) each storing more than two possible data states, wherein each data state is represented by two or more data bits and the respective data bits are classified into two or more groups (or sets), and by storing two or more groups of parity bits corresponding to the two or more groups of the data bits respectively into a plurality of second memory cells (single bit memory cells or multibit memory cells). The memory devices include a plurality of sense amplifiers for sensing the two or more groups of the data bits and a plurality of data latches for latching the two or more groups of the sensed data bits, respectively. Each of the sense amplifiers corresponds to at least two of the data latches depending upon bits per cell, and the plurality of the data latches are classified into two or more groups each including only one of the at least two data latches corresponding to each sense amplifier. In particular, the memory devices include an ECC circuit which checks error bits out of the latched data bits sequentially by the group and corrects the checked error bits sequentially by the group.

Refine Search

Search Results -

Terms	Documents
L16 same L12	3

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L17

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, January 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L17	L16 same l12	3	L17
L16	correct$ near4 writing	2322	L16
L15	L14 same l9	28	L15
L14	correct$ same writing	10461	L14
L13	L12 and l11	24	L13
L12	l9 same writ$	120	L12
L11	L9 same test$	35	L11
L10	L9 same bisr	0	L10
L9	L8 same memory same cell	289	L9
L8	ecc same correct$	5253	L8
L7	L6 same cell	18	L7
L6	L5 same memory	27	L6
L5	L4 same l3	30	L5
L4	error	376725	L4

L3	bisr	72	L3
L2	L1 same memory	40	L2
L1	ecc same repair	66	L1

END OF SEARCH HISTORY

L24: Entry 7 of 24 File: USPT May 2, 2000

DOCUMENT-IDENTIFIER: US 6058047 A
TITLE: Semiconductor memory device having error detection and correction

CLAIMS:

12. A method of writing/reading data with regard to a semiconductor memory having a memory region divided into a plurality of blocks including backup blocks, the number of times data is written to each block being limited,

said method comprising the steps of:

reading data from said semiconductor memory;

performing an error-check on the read data for each block;

counting only the number of correctable errors detected by the error check of the read data, for each block and rewriting the data of a corresponding block to at least one of said backup blocks when the number of errors detected reached a preset value; and

inhibiting reuse of said block as a defective block.

13. The method according to claim 12, wherein a plurality of main blocks each having data to be subjected to an error-check, and a plurality of flash memories are used as said semiconductor memory.

Refine Search

Search Results -

Terms	Documents
L28 same identical	14

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L30

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Wednesday, January 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L30	l28 same identical	14	L30
L29	L28 same cell	36	L29
L28	l26 same block	196	L28
L27	L26 same sequentially	25	L27
L26	L25 same memory	537	L26
L25	ecc adj3 circuit	1035	L25
L24	l18 same block	24	L24
L23	L18 same memory	14	L23
L22	L21 same memory	4	L22
L21	l18 same l19	11	L21
L20	L19 near4 l18	6	L20
L19	circuit	961546	L19
L18	error-check	162	L18
L17	L16 same l12	3	L17

L16	correct$ near4 writing	2322	L16
L15	L14 same l9	28	L15
L14	correct$ same writing	10461	L14
L13	L12 and l11	24	L13
L12	l9 same writ$	120	L12
L11	L9 same test$	35	L11
L10	L9 same bisr	0	L10
L9	L8 same memory same cell	289	L9
L8	ecc same correct$	5253	L8
L7	L6 same cell	18	L7
L6	L5 same memory	27	L6
L5	L4 same l3	30	L5
L4	error	376725	L4
L3	bisr	72	L3
L2	L1 same memory	40	L2
L1	ecc same repair	66	L1

END OF SEARCH HISTORY

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L17: Entry 3 of 3 File: USPT Jul 19, 1983

DOCUMENT-IDENTIFIER: US 4394763 A

**** See image for Certificate of Correction ****

TITLE: Error-correcting system

Brief Summary Text (10):

Regarding the above mentioned 2-bit errors, the 2-bit errors may be classified into wo modes or types. In a first mode or type, the 2-bit errors comprise both a first 1-bit soft error and a second 1-bit soft error both in different words. In a second mode or type, the 2-bit errors comprise both a 1-bit hard error and a 1-bit soft error. With regard to the first mode, it is easy for the ECC logic circuit to correct such 2-bit soft errors that occur in different words. This is because, as previously mentioned, the soft error does not occur repeatedly in the same memory cell. Accordingly, if the ECC logic circuit detects each soft error in one of the words and corrects the same, thereafter, the data at the corresponding memory cell can be corrected by writing the corrected data again into the same memory cell. Alternately, such soft error can also be corrected by the ECC logic circuit. That is when the ECC logic circuit detects such soft error in one of the words during an ordinary memory accessing operation, the ECC logic circuit can correct the same by rewriting the corrected data again into the same memory cell. Further, it may also be possible for the ECC logic circuit to, first scan with a certain period the memory device and read the data of all the addresses thereof sequentially, and then, if the soft error in one of the words is found, rewrite the corrected data again into the same memory cell.

L11: Entry 34 of 35 File: USPT Feb 16, 1988

DOCUMENT-IDENTIFIER: US 4726021 A
TITLE: Semiconductor memory having error correcting means

Detailed Description Text (30):
Checking or testing the memory after it is manufactured in accordance with this invention, includes various kinds of tests including a test for an error correcting function. In testing the semiconductor memory, it is specifically pointed out that it has a built-in error correcting function. However, if for example a single-error correcting code is used as an ECC and the memory accidentally has a defect (hard error) in one memory cell, then in this case the defect cannot be found because the readout data is corrected by the ECC, thus resulting in an apparent error-free memory.

Detailed Description Text (33):
The present invention seeks to solve this problem and provide a semiconductor memory having a built-in error correcting function using an ECC, which can test the memory cells per se for storing redundant bits of the ECC, i.e., check bits, encoding circuit, decoding circuits and the like, independently of each other.

Detailed Description Text (100):
As described, according to the present invention, in a semiconductor memory having a built-in error correcting function, writing in the memory cells for storing check bits for an ECC is performed using input data from terminal D.sub.in or data generated by an encoding circuit. On the contrary, reading data from the memory array is performed by switching between the operation and non-operation of error correction by a decoding circuit and by switching between the output and non-output of check bits. As a result, independent tests are possible, such as a test for memory cells for check bits, a test for the encoding circuit and a test for the decoding circuit.